Report for Session 2: Electronics & Associated Software Activities
Prior to Baseline Review
Pixel Detector

Major Milestones:
- o FPIX2 readout chip: Irradiation tests on pre-FPIX2 chips to study Single Event Effects (SEE); design and submission of FPIX2
- o Pixel control and readout options: Decision on the baseline scheme
- o EMI effects: Understand the effect and study various shielding and grounding options
- o Multi-chip-module: Assemble and test of first five-chip module using FPIX1 and new high density interconnect
- o Plane demonstrator
- o PCI based test-stand completed

Schedules:
FPIX2 Readout Chip Development:
- o Pre-FPIX2_I: Irradiation tests   Dec. 2000
- o Pre-FPIX2_TB: bench tests   Dec. 2000 – Jan. 2001
  - ▪ Irradiation tests   Feb./March 2001
  - ▪ Detector test   Summer 2001
- o FPIX2: Submission   4th quarter 2001

Pixel Control and Readout Options:
- o Understand radiation level and effect on COTs   April 2001
- o Decision on the readout scheme   June 2001

EMI tests:
- o Results and solutions   May 2001

Multi-Chip-Module:
- o Assembly ready for test   June 2001
- o Tests   July/August 2001

Plane Demonstrator:
- o Assembly ready for test   September 2001
- o Tests   Last quarter 2001

PCI-Based Test Stand:
- o Ready for testing(hardware and software)   Feb. 2002

Development and/or Test beam Electronics and Associated Software:
❖ **Tests:**
  ➢ Bench tests, irradiation tests, source tests (with detectors)

- ➢ Beam test: Since it's unlikely that there'll be a test beam available at BNL, the earliest possible time for a beam test will be Jan./Feb. 2002. We may either use our existing silicon strip telescope or move to a new pixel detector telescope.

- ❖ **Needs:**
  - ➢ EMI effects: Solutions, controller/readout board, buffer board that may require radiation tolerant components; high density interconnect
  - ➢ Commercial electronics
  - ➢ Test-stand software
  - ➢ Test-stand; data-combiner board
  - ➢ Personnel and resources: Continued support from Fermilab engineers (CD/ESE, PPD/ESD) and computing professionals

Custom ICs:
- ❖ **FPIX2 should be available by the time of the baseline review**

BTeV Standard Test Stands:
- ❖ Pixel will be the first group to use the new PCI-based test-stand

Simulations of Electronics:
- ❖ Models, analysis and simulations
  - ▪ Architecture, readout bandwidth required, pixel size, possible causes of data losses and the rate of data loss.

Pixel Readout:
- ❖ Away from the baseline design: We are presently considering three different options to control the pixel readout chips and readout the pixel data. These are:
  - ➢ All the communication with the pixel module us done by fiber optics. The FPIX control/monitoring ASIC, data serializer and opto-electronics (fiber optics, VSECL, PIN diodes etc) are assembled directly on the pixel module. All components need to be low mass and radiation hard. This is the baseline scheme described in the Proposal.
  - ➢ The pixel module communicates through LVDS signals produced by the FPIX2 chips with a controller/data readout board located far enough outside the vacuum enclosure. Fiber optics is then used to interface the controller board with the DAQ. The radiation at 25.4cm from the beam line is expected to be 15 Krad at our designed luminosity. Either we have to move the controller board further away or we have to use radiation tolerant Components-off-the-shelves (COTS). Still there is the suspicion that single event upsets (SEU) can interfere with the phase locked loops (PLL) of the high-speed serializers for data transmission to the data acquisition system.
  - ➢ In this option, it's envisaged that the chip will drive high-speed LVDS signals over copper to about 3m away from the pixel module. Possibly, some buffering devices will sit about 30cm from the pixel module, outside the vacuum enclosure. These devices will transform the LVDS non-return-t0-zero signals to AC balanced and buffer the rest of the way to the controller/data readout/combiner

board. This option is considerably simpler to implement. It may however, be more susceptible to EM pick-up from the beam.

❖ We plan to do tests on the EMI effects that will help us to decide which is the best scheme to pursue.

Data Controller/Compression IC:

❖ With option b) or c), we don't need a data controller IC. In any case, we don't think we need such an IC for the baseline review even if we were to adopt option 1) above.

RF Pickup:

❖ We will do tests to measure the performance of the FPIX1 chips with different lengths of the differential readout and control cable. Different shielding, power supply and grounding scheme will also be tested.

Grounding:

❖ To be studied as part of 'RF Pickup'

Electronics Outside The Vacuum Vessel:

❖ Radiation level: We expect this will be studied during the next 3 months
❖ Use of COTS: Depending on the radiation level, we may have to use radiation tolerant parts or move the buffer/controller board further away from the beam

Secondary Event Upsets (SEUs):

❖ These will be studied during the next three to four months with pre-FPIX2 chips